FAMU/FSU College of Engineering

Department of Electrical and Computer Engineering

Functional Decomposition

Team 303 Software Defined Radio

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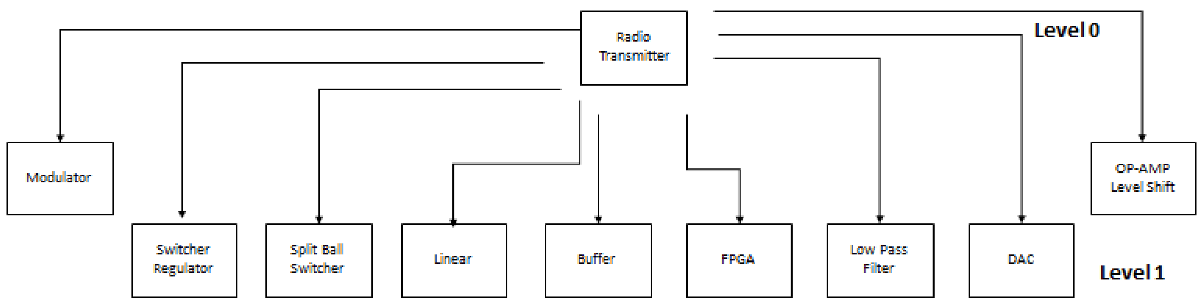
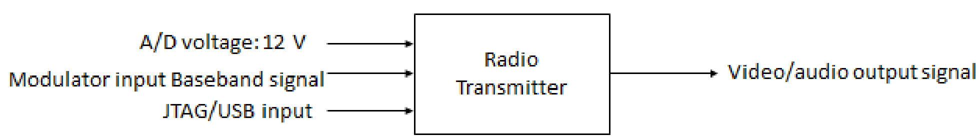
The functional decomposition is on a radio transmitter exciter with three inputs and one output. The main purpose is to design a higher frequency signal of the video/audio input.

Function Tree



Level 0: Radio transmitter

Module	Radio transmitter exciter
Inputs	JTAG/USB input data Power: 12 V (digital or analog) Modulator input baseband signal
Outputs	Video/audio output: ± 2 fin fm
Functionality	Create a higher frequency signal of the video/audio signal input. (add more)



Level 1: Switcher Regulator

Module	Switching Regulator
Inputs	Power: 12 V Digital/Analog
Outputs	Power: 1.2 V, 3.3 V and 5.0 V
Functionality	Switching regulators take the input signal (both digital and analog) and convert it to a lower voltage level for use with the electronics (FPGA and DAC).

Level 1: Linear Regulator

Module	Linear
Inputs	Power: ± 5 V
Outputs	Power: ± 3 V, 3.3 V
Functionality	Take in Power and decrease the right amount of voltage for each component.

Level 1: Split Ball Switcher

Module	Split Ball Switcher
Inputs	Power: 12 V (Analog)
Outputs	Power: ± 5 V
Functionality	Take in the 12 V and convert into ± 5 V for the positive and negative power supply in the op-amps.

Level 1: Oscillator

Module	Oscillator
Inputs	Power: 3.3 V
Outputs	Sinusoidal Wave signal: 100 MHz with 50 mV PP
Functionality	The oscillator will take the signal from one of the digital 3.3V regulators and create a signal which can be used by the FPGA as a form of clock.

Level 1: Buffer

Module	Buffer
Inputs	Sinusoidal Wave signal: 100 MHz with 50 mV PP
Outputs	Sinusoidal Wave signal: low current 100 MHz signal
Functionality	The buffer will make sure the oscillating signal used for the clock draws low current in an attempt to reduce effects of the load (FPGA) on the source.

Level 1: FPGA

Module	FPGA
Inputs	Sinusoidal Wave signal: low current 100 MHz signal JTAG/USB input
Outputs	Data designated by the user
Functionality	The FPGA is the means of interaction with the user. It can take in different forms of data (through the use of different instruments and the JTAG/USB) and transmit it to the DAC.

Level 1: DAC

Module	DAC
Inputs	Data from FPGA
Outputs	Analog Signals: I and Q
Functionality	The DAC takes in data from the FPGA and converts it into two different analog signals, I and Q. The in-phase (I) signal is identical to the quadrature (Q) in both magnitude and frequency, the only difference being their phase. The reason for the two signals instead of one, has to do with the difficulty of creating a circuit which modulates a high frequency wave (the carrier wave) with a message input signal. To get around this, you can use these two signals to get the same effect as direct phase manipulation.

Level 1: OP-AMP level shift

Module	OP-AMP level shift
Inputs	Power: ± 3 V Analog Signal
Outputs	Amplify Analog Signal
Functionality	The op-amps take the I/Q signals and amplify the voltage to a suitable level for the modulator.

Level 1: Low Pass Filter

Module	Low Pass Filter
Inputs	Analog Signal
Outputs	Filtered Analog Signal (fm(I) & fm(Q))
Functionality	Two low-pass filters (LPFs) are used to get rid of the high frequency of the signal coming from the op-amp, as they are largely un-needed and contain no important data.

Level 1: Modulator

Module	Modulator
Inputs	Filtered Analog Signal Modulator input baseband signal
Outputs	Video/audio output: ± 2 fin fm
Functionality	The modulator takes the I/Q signals and convolves with a high-frequency carrier signal to create a higher frequency signal that still contains the data from the I/Q signal. The benefit of using a higher-frequency signal is on the transmission side of things. Higher frequency waves dissipate less power, travel further than low-frequency waves, and require smaller antennas to transmit them.

Software Radio Transmitter