

# **FAMU/FSU College of Engineering**

## **Department of Electrical and Computer Engineering**

### **Targets**

**Team 303 Software Defined Radio**

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## **Targets for functions**

The 1.2V, 3.3V, and 5.0V regulators (both switcher and linear) used in the design of the system will be composed of the same component. Based on the component datasheet provided by Texas Instruments, the input signal of the regulators should fall between 4.5V - 17V, which our input signal of 12V falls well within. The outputs of the regulator will produce our desired voltage of either 1.2V, 3.3V, or 5.0V and the analog signals can be tested with the use of a simple voltage probe or multimeter.

The oscillator component will produce a 100MHz signal from the 3.3V regulator which will provide the FPGA with an input clock signal. This clock speed was designated by the FPGA's manufacturer Texas Instruments and is found in the component datasheet. The oscillator will be supported by the buffer which will reduce the current to a suitable level for the FPGA as well as help keep the functions of the FPGA working at the same frequency.

The FPGA which will be used for the design requires a 1.2V supply input, which is going to be directly obtained from the output of the regulators. The datasheet provided by Texas Instruments states that the operating range of the FPGA has a marginal value of 1.14V - 1.26V ( $\pm 5\%$ ).

The DAC takes in 8-bit output of the FPGA as well as both analog and digital input signals at a range of 2.7V - 3.6V. This range was specified by the component datasheet and the 3.3V regulator used in the design falls well within this input range.

For the basic electrical components found at the end of the design, the op-amps have a slew rate of 2500 V/ $\mu$ s, which is plenty responsive enough for the system in place, as the design requires less than a tenth of a percent of that voltage and the frequency is only 3 magnitudes slower than that rate. The low-pass filters have a cutoff frequency of 30 MHz, which will chop off the undesirable high frequency output of the op-amps.

## **Testing**

A multitude of different softwares will be used for simulation and testing of various circuits and code. MATLAB will be heavily used in development of the signal processing. Other softwares like LTSpice and ADS will provide useful tools for analyzing the circuit/PCB board. The design/layout of the PCB board itself will be created through KiCad. The 100 MHz clock and input to the system will be provided through the FPGA and the Vivado software. Tina (TI) will also be used for simulation of analog circuits.

## Summary

Metric No.	Need	Metric	Imp.	Units	Marginal Value	Ideal Value
1	Reprogrammable (multi-channel, multi-bandwidth)	Binary	1	Yes/No	Yes	Yes
2	Inexpensive and commercially available parts	Amount	2	Dollars	?	<\$3000
3	Schematic/Board layout	Binary	3	Yes/No	Yes	Yes
4	KiCad Schematic/Board layout	Binary	3	Yes/No	Yes	Yes
5	All components capable of high fidelity, competitive with current standards	Frequency	1	MHz	60Hz	100MHz
6	On board flash memory integrated with FPGA (JTAG and USB) (256 8-bit digital words)	Memory (RAM)	1	Byte	500000-600000	589824 (FPGA specific)